OVERVIEW

EverOn™ is the 'Always On' solution for 'ultra-low power designs with a wide operating voltage range. EverOn provides read/write access down to the bit cell retention voltage, 0.6V in 40ULP and 22ULL, and 0.63V in 28HPC+ process nodes. It delivers up to 70% dynamic power savings and up to 60% static/leakage power savings compared to foundry and other SRAM solutions.

sureCore provides best-in-class power savings by augmenting standard foundry memory 6T bit cells with its innovative, patented architecture, powerful compiler technology and a set of finely grained sleep modes.

Product development includes the implementation and execution of a comprehensive verification and characterization strategy.

Detailed datasheets spell out power, performance and timing data covering all process corners across a wide operating voltage range. The full industrial temperature range of -40C to 125C is supported.

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PRODUCT FEATURES

EverOn™ is designed with a rich set of innovative features and functions that contribute to significant power savings.

- Single port, single voltage rail synchronous SRAM
- Hierarchical Bit Line Architecture – sub-diving the array into columns/ rows, banks and local blocks
- 'Smart Assist' – controls voltage drive to selected bit cells and bit lines in read and write cycles
- Pre-charge mux sense – read circuit that helps reduce both active and leakage power in the memory array
- SVT Periphery – enables higher performance at low operating voltages
- Configurable global data mux sets column length and overall aspect ratio
- Programmable sleep modes: Light Sleep, Deep Sleep (data retention), Shutdown, configurable on an individual bank basis, up to 4 banks supported
- Configurable word length from 16 to 72-bits
- 576Kbit max instance size. Configurable – 8KX72, 16Kx36
- APTG and BIST support
- Supports industry standard EDA design flows
- Operating voltage down to the bit cell retention voltage

ADVAN ED SLEEP MODES

EverOn mes complete with a rich set of user-programmable sleep modes. Each SRAM is divided into four banks, all inde ndently controllable as either active, sleep (retained) or off. This allows one or more memory banks to be shut down, c ating additional power savings without splitting one large memory into several smaller instances. In addition, the peri ery can be placed into low power mode to achieve even lower power consumption.

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