OVERVIEW

PowerMiser™ is the ideal single-port synchronous low-power SRAM IP for energy e□cient SoC systems in a wide range of market applications.

It reduces dynamic power by up to 50% and static/leakage power by up to 20% compared to foundry and other SRAM solutions. It delivers these

PRODUCT FEATURES

PowerMiser™ architecture supports a rich power savings and functional feature set:

- Single port, single voltage rail synchronous SRAM
- Hierarchical Bit Line – subdividing the array into columns/ rows, banks and local blocks.
- Configurable mux factor sets column length and overall aspect ratio
- Bit Line Voltage control eliminates potential low operating voltages issues
- Enable only required local block word line and bit line drivers
- SVT, HVT, UHVT periphery
- Operating voltage: 0.9V +/-10% in 28nm, 0.8v +/-10% in 22nm
- Retention voltage: 0.55V in 28FDSOI, 0.63V in 28HPC+, 0.6V in 22ULL
- Configurable word length, up to 144 bits
- Configurable 32 or 64 bit lines
- Programmable sleep modes: Light Sleep, Deep Sleep (data retention), Shutdown
- 576Kbit max instance size. Configurable – 4Kx144, 8KX72, 16Kx36
- APTG and BIST support
- Supports industry standard EDA design flows

RIGOROUS VERIFICATION

sureCore's extremely rigorous verification strategy includes silicon validation, high sigma statistical analysis, and identifying and analysing key design parametrics. This supplements a qualification regime that includes an industry-standard 125°C, 1,000-hour High Temperature Operating Life (HTOL) test that, to date, every device has passed! Statistical analysis covers PVT extremes with readability, writability and access disturb margins validated at 6σ. An extensive Monte Carlo simulation of specific design parameters, validated across the full PVT space, assures robust operation. A thorough physical verification suite including IR drop, EM and crosstalk checks augment this regime.

SRAM CHARACTERISATION STRATEGY

sureCore has invested heavily in leading edge tooling to build an extensive and automated SRAM characterization environment that accurately determines all timing arcs across a full range of operating corners. This is key to achieving outstanding EDA model accuracy.

COMPILER SUPPORT

sureCore's SRAM technology makes scalable memory a priority. It's low power operation techniques do not rely on detailed tuning and are suitable for of many different capacity and word length memories.

sureCore's memory compiler supports capacities ranging from 8Kbit to 576Kbit and provides a tool for the rapid estimation of power, area, and performance, as well as the generation of fully characterised memory instances. sureCore memories easily integrate into typical SoC design flows through compiler generated industry-standard simulation, layout, timing analysis and DFT views.

SUMMARY

sureCore's PowerMiser™ revolutionizes low power SRAM design by delivering dramatically improved dynamic power characteristics coupled with significant static power savings.

WHEN POWER IS PARAMOUNT

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