

OVERVIEW

Today's emerging markets aren't playing by yesterday's rules... design or otherwise. SoC architects developing cutting edge artificial intelligence, imaging, machine learning, wearable, and IoT devices can no longer make do with standard memory IP to deliver lower and lower power targets. Their designs are ahead of the game. They demand application specific power and performance targets that demand "out-of-the-box" thinking, targets that deliver market leading energy efficiency.

When developers need extraordinary Ultra-Low Power Memory IP they turn to SureFIT™, sureCore's application-centric custom memory design service to deliver on their unique design and PPA requirements. Memory tuned to their low-power needs. Memory tuned to deliver disruptive innovation. Memories that are optimised, verified, characterised and ready for integration.

PROVEN TECHNIQUES

SureFIT deploys silicon proven and patented low-power design techniques with powerful verification and characterization methodologies to deliver optimal memory solutions.

Customers come seeking many attributes including multiple read/write ports, burst capabilities, ultra-low leakage retention modes, low dynamic power, near-threshold operation, write masking and BIST/DFT support. Memory tuned to their precise requirements. Memory tuned to deliver the target performance demanded by next generation products.

SureFIT develops memory variants including SRAM and Register Files and can be based on either standard foundry or custom bit cells. Foundry bit cells deliver the highest possible density; while custom bit cells, built according to standard process rules, deliver Ultra-Low voltage operation.

SureFIT applies patented proven design techniques and innovative memory architectures including:

- Segmented arrays and bit line voltage control to deliver optimal dynamic power and performance
- SMART-Assist circuitry to deliver robust near-threshold operation across process and temperature extremes
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