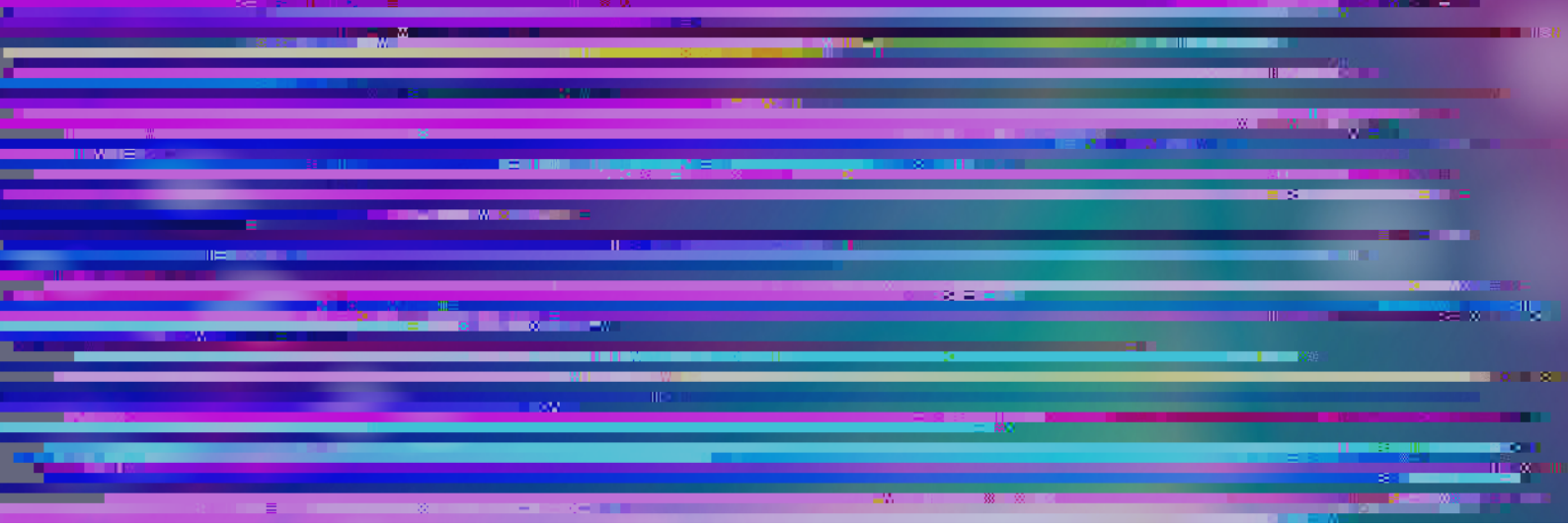

WHEN LOW POWER IS PARAMOUNT

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The ability of a memory (SRAM or register file) to operate at reduced voltage is normally limited by the bit cell ς the basic data storage element (see Figure 1). Especially in the case of the 6T bit cell that is used in SRAM, the trade-offs made in the bit cell in order to enable it to reliably store data, to be read from, and to be written to, usually result in there being a limited voltage range over which the bit cell will operate. There are two basic ways to extend the operating range to enable low-voltage operation:

Hierarchical partitioning of long wires with high capacitance, such as bit lines. Partitioning of these wires reduces the

Third party benchmarking has indicated that sureCore register files can deliver very significant power savings compared to more traditional register file designs. In particular dynamic power savings in the region of 75% can be shown. Furthermore, the capability to operate over a wide voltage range means that both typical and low power operating modes of an SoC may be optimised.

This paper explains how sureC2WSa specialised low-power register file design is optimised to achieve both low operating voltage and low power consumption. This architecture significantly eases integration with low voltage on-chip. This was achieved by:

- Using a custom bit cell, with separately optimised read and write ports, that is designed to work at low voltage,
- Using our existing low-power SRAM design techniques to reduce active power in the periphery circuits, and
- Adding additional register file specific optimisations to further reduce activity on the register file bit lines.

For many applications cutting power is the #1 priority ç even often at the expense of area. In these cases, reviewing the contribution made to overall consumption by register files can be an illuminating analysis. The sureCore low power register file provides a welcome addition to the system designers battle to reduce power.

sureCore ç When Power is Paramount.